TUTORIAL-3

Q-1:-A register is defined as _____

a) The group of latches for storing one bit of information
b) The group of latches for storing n-bit of information
c) The group of flip-flops suitable for storing one bit of information
d) The group of flip-flops suitable for storing binary information

Answer: d

Explanation: A register is defined as the group of flip-flops suitable for storing binary information. Each flip-flop is a binary cell capable of storing one bit of information. The data in a register can be transferred from one flip-flop to another.

Connecting Registers - Bus Transfer

- For a bus system to multiplex k registers of n bits each
  - No. of multiplexer = n = No. of bits
  - Size of each multiplexer = k x 1, k data lines in each MUX

- **Construction of bus system for 8 register with 16 bits**
  - **16 bit register X 8**
  - **16 MUX 8X1 multiplexer—— NO OF MUX REQUIRED**
  - **Bus selection S0, S1, S2**

Q2-A Digital computer has a common bus system for 16 registers of 32bits each.

(i)How many selection inputs are there in each multiplexer ?

(ii)What size of multiplexer is needed

(iii)How many multiplexers are there in a bus ?

(iv)How many data lines are there in each multiplexer?

Notes

Common bus system for 16 registers of 32 bits each.

(I) How many selection inputs are there in each MUX?

Soln:- 2^x = no. of registers

$\Rightarrow x$ selection inputs of each MUX

$\because 2^x = 16$

$\Rightarrow$ Here, $x = 4$

$\therefore$ 4 selection inputs lines in each MUX

(II) What size of MUX needed?

Soln:- Size of MUX = Total no. of registers X1

= 16 X1

$\therefore$ 16X1 MUX

(III) How many multiplexers are there in a bus?

Soln:- No. of MUX = bits in each register = 32

$\therefore$ 32 MUX are needed in a bus.

(IV) How many data lines in each multiplexer?

Soln:- data lines = Input lines in each MUX

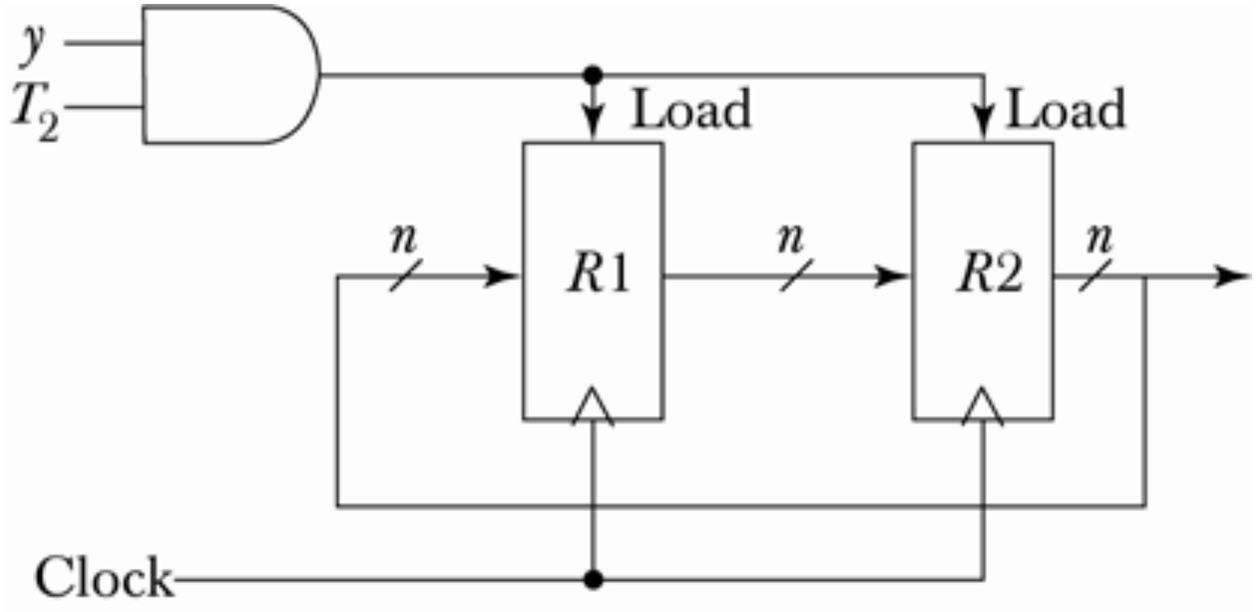
Size of MUX = 16 X 1

$\therefore$ 16 data lines in each MUX.

- Q3—-Show by hardware implementation:

yT_2 : R2<- R1, R1<- R2

Answer-2



QUESTION-4:-

The 8 bit register AR,BR,CR,DR initially have the following values
DR---11101010
AR---11110010
BR---11111111
CR---10111001
Determine the 8 bit values in each register after the execution of the following sequence of micro-operations
AR<---AR+BR
CR<-----CR ^ DR, BR<-------BR+1
AR<-------AR-CR

AR = 11110010 CR = 10111001

BR = 11111111 DR = 11101010

AR ← AR + BR

```
  AR = 11110010
  BR = 11111111 +
  ------------
new AR = 11110001
```

CR ← CR ∧ DR

```
  CR = 10111001
  DR = 11101010  ∧ (AND)
  ------------
new CR = 10101000
```

BR ← BR + 1

```
  BR = 11111111
       +      1
  ------------
new BR = 00000000
```

AR ← AR − CR

new AR new CR

{ Because every micro-operation execution is in sequence. means one after another }

```
  AR = 11110001
  CR = 10101000 −
  ------------
```

Subtraction with (A + B̄ + 1) method

so AR − CR

⇒ AR + C̄R + 1


```
  CR = 10101000
  C̄R = 01010111
       +      1
  ------------
       01011000
```

AR + C̄R + 1

∴ AR → 11110001

C̄R + 1 → 01011000 +

01001001

finally, AR = 01001001

∴ AR ← AR − CR.

Q-5:-

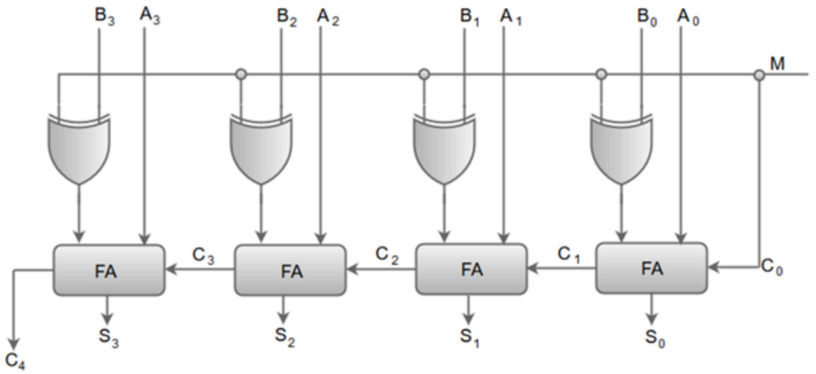
What are the three output conditions of a three-state buffer?

a) HIGH, LOW, High-Z
b) High-Z, 0, float
c) Negative, positive, 0
d) 1, Low-Z, float

Q6- The 4 bit adder subtractor circuit has the following values for input mode M and data inputs A and B . In each case , determine the values of the outputs- $S_3S_2S_1S_0$ and C_4

	M	A	B	$S_3S_2S_1S_0$	C_4
I	0	O111	O110		
II	0	1000	1001		
III	1	1100	1000		
IV	1	0101	1010		
V	1	0000	OOO1		
VI	1	O100	OOO1		
VII	0	OO10	OO10		
VIII	1	O110	O100		
IX	0	OO10	O110		
X	1	O101	10		

4 bit adder-subtractor:



SOLUTION

	M	A	B	$S_3S_2S_1S_0$	C_4
I	0	O111	O110	1101	0
II	0	1000	1001	OOO1	1
III	1	1100	1000	O100	1
IV	1	0101	1010	1011	0
V	1	0000	OOO1	1111	0
VI	1	O100	OOO1	OO11	1
VII	0	OO10	OO10	O100	0
VIII	1	O110	O100	OO10	1
IX	0	OO10	O110	1000	1
X	1	O101	10	OO11	1

Q-6:-

Which micro operations carry information from one register to another:

a. Register transfer
b. Arithmetic
c. Logical
d. All of these

Q-7:-

Micro operation is shown as:

a. R1→R2

b. R1←R2

c. Both

d. None

Q-8:

Which operation is binary type, and are performed on bits string that placed in register:

A- Logical micro operation
B- Arithmetic micro operation
C- Both
D- None

Q9-A Digital computer has a common bus system for 4 registers of 2 bits each.

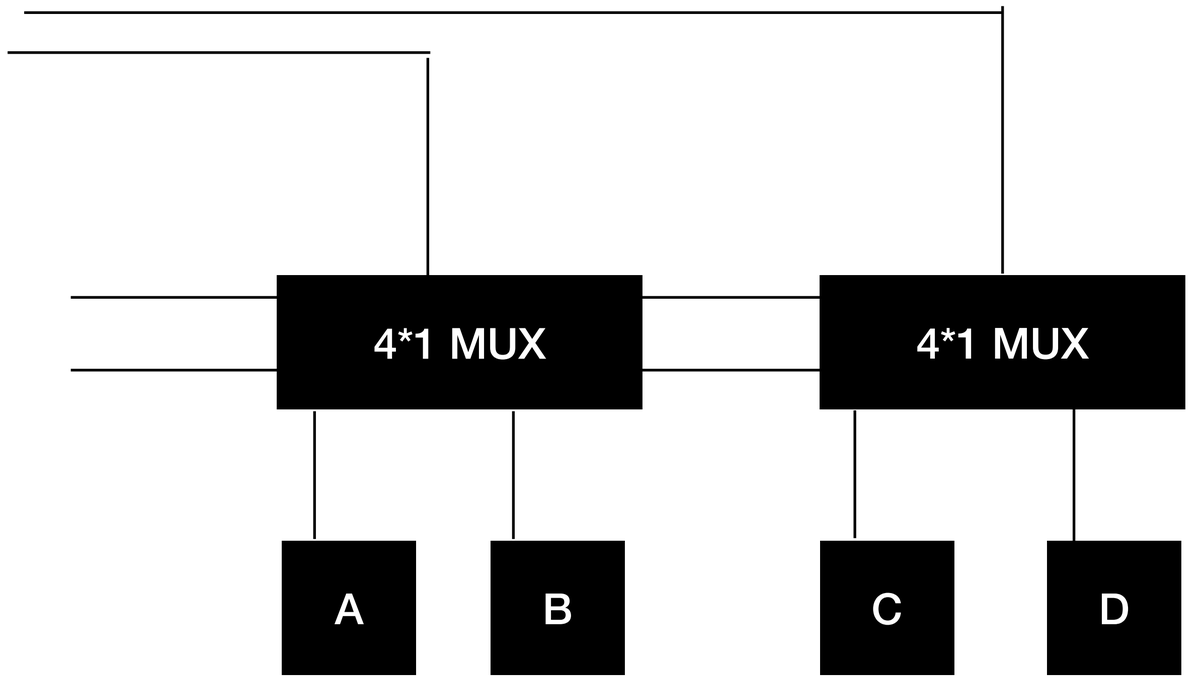
(i)What size of multiplexer is needed ?

(ii)How many multiplexers are there in a bus ?

(iii)How many data lines in each multiplexer?

(iv)How many selection inputs are there in each multiplexer ?

(v) DRAW block diagram of required common bus using MUX, along with function table



FUNCTION TABLE

S_1	S_0	Register
0	0	A
0	1	B
1	0	C
1	1	D

COMPLETE DIAGRAM YOURSELF